AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently amended) A method, comprisinges the steps of:
transferring a data block between a flash memory and a memory controller; and
computing an ECC for said data block while transferring the data block.

2. (Original) The method of claim 1, wherein transferring the data block comprises transferring the data block between a NAND Flash memory and the memory controller.

3. (Original) The method of claim 1, further comprising:
storing a first portion of the ECC in a first register; and
storing a second portion of the ECC in a second register if the first register is full.

4. (Original) The method of claim 3, wherein storing in a second register comprises selecting the second register using a switching mechanism.

5. (Original) The method of claim 1, wherein computing the ECC comprises performing the exclusive-or function.

6. (Currently amended) A system, comprising:

a flash memory;

a controller coupled to the flash memory; and

~~at least one register coupled to the controller;~~

wherein said controller shifts a data block between the flash memory and the controller while computing an ECC for said data block.

7. (Original) The system of claim 6, wherein the flash memory is a NAND Flash memory.

8. (Original) The system of claim 6, further comprising:

storing a first portion of the ECC in a first register; and

storing a second portion of the ECC in an alternate register if the first register is full.

9. (Original) The system of claim 8, wherein the controller transfers contents of all registers to memory if all registers are full.

10. (Original) The system of claim 8, further comprising a switch to select the alternate register.

11. (Original) The system of claim 6, wherein computing the ECC comprises performing the exclusive-or function.

12. (Currently amended) A system comprising:

a means for storing a data block;

a means for controlling ~~transferring a~~ the data block;

a means for ~~simultaneously~~ computing an ECC of the data block; and

a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block.

13. (Original) The system of claim 12, wherein the means for storing is a NAND Flash memory.

14. (Original) The system of claim 12, further comprising:
storing the ECC in a first register; and
storing the ECC in an alternate register if the first register is full.

15. (Original) The system of claim 12, further comprising transferring contents of at least one register to memory if all registers are full.

16. (Original) The system of claim 14, further comprising a switch to select the alternate register.

17. (Original) The system of claim 12, wherein computing the ECC comprises performing the exclusive-or function.

18. (Currently amended) A memory controller adapted to couple to a memory, comprising:
a memory interface; and
an ECC engine that computes an ECC~~; wherein the ECC engine computes an ECC~~ while transferring a data block between the ECC engine and memory.

19. (Original) The memory controller of claim 18, further comprising:
a switching mechanism coupled to the ECC engine; and
a register bank coupled to the switching mechanism, comprising at least one register;
wherein the ECC engine stores the ECC in a register selected by the switching mechanism, the register having space available for ECC storage.

20. (Original) The memory controller of claim 18, wherein transferring a data block comprises transferring the data block between the ECC engine and a flash memory.

21. (Original) The memory controller of claim 18, wherein transferring a data block comprises transferring the data block between the ECC engine and a NAND Flash memory.

22. (Original) The memory controller of claim 18, wherein the ECC engine transfers a data block by reading the data block from memory.

23. (Original) The memory controller of claim 18, wherein the ECC engine transfers a data block by writing the data block to memory.

Please add the following new claims:

24. (New) The system of claim 8, wherein the first register is in the controller.

25. (New) The system of claim 8, wherein the alternate register is in the controller.

26. (New) The system of claim 10, wherein the switch is in the controller.